A High Speed Programmable Ring Oscillator Using InGaZnO Thin-Film Transistors

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***Abstract*—This paper presents a high speed digitally programmable Ring Oscillator (RO) using Indium-gallium-zinc oxide thin-film transistors (IGZO TFTs). Proposed circuit ensures high speed compared to the conventional ROs using negative skewed scheme, in which each inverter delay is reduced by pre-maturely switching on/off the transistors. In addition, by controlling the load capacitance of each inverter through digital control bits, a programmable frequency of oscillation was attained. Proposed RO performance is compared with two conventional designs under same conditions. From simulation, it has been observed that the proposed circuit has shown a higher frequency of oscillations (283 KHz) compared to the conventional designs (76.52 KHz and 144.9 KHz) under same conditions. Due to the programmable feature, the circuit is able to generate 8 different linearly spaced frequencies ranging from 241.2 KHz to 283 KHz depending upon three digital control bits with almost rail-to-rail voltage swing. The circuit is a potential on-chip clock generator in many real-world flexible systems, such as, smart packaging, wearable devices, RFIDs and displays that need multi frequencies.**

***Keywords*—Oxide TFTs, High speed programmable RO, negative skewed and rail-to-rail logic.**

I. INTRODUCTION

Amorphous Oxide thin-film transistor (TFT) technology is gaining significant interest due to its ability to provide transparent and flexible electronics at low cost with good stability [1] and improved performance compared to other competing TFT technologies like organic and a-Si:H. Oxide TFTs find potential applications not only in display backplanes, but also in RFID tags [2], NFCs [3], data converters [4], smart packaging, biomedical [5]. However, lack of stable complementary type transistor (p-type) makes circuit design difficult, which is essential in building complete systems with this technology. Since CMOS design cannot be adapted directly, new circuit techniques have been developed to overcome this challenge [6][7][8].

Oscillators play a vital role as an on-chip clock generator in many circuits or systems, namely, data converters, DC-DC converters and wearable devices. Ring Oscillator (RO) is a simple vehicle to obtain multi-phase clock signals. Applications like RFIDs, NFCs, and wearable systems (mainly ADCs) need clock signals with frequency at least in the order of hundreds of kilo-hertz. However, it should be noted that amorphous nature of the semiconductor in IGZO TFTs limits the mobility of the transistors and hence, the operating speed of circuits. Literature [9]-[14] reports ROs in oxide TFTs but, due to limited voltage swing, they are not suitable as on-chip clock generator. Moreover, oscillators in [15],[16] are able to demonstrate full voltage swing but [15] has limited speed even though individual TFTs are showing a relative high mobility of 36 cm^2/V.s and [16] employs dual-gate devices demanding more processing steps compared to single gate counterpart. In addition, all the designs are limited to generate a single frequency of oscillation. A voltage controlled oscillator (VCO) [17] demonstrates frequency of oscillations ranging from 400 Hz to 560 Hz, proportional to input control voltage. However, this frequency is quite low for afore-mentioned applications.

In order to address all the above challenges for a given technology, this work proposes a novel high speed RO that can ensure complete rail-to-rail operation with programmability (eight linearly spaced different frequencies). The proposed RO is able to demonstrate high frequency of oscillations using negative skewed delay scheme [18]. This technique reduces propagation delay of single stage inverter by prematurely triggering transistors. Since the output frequency of RO is inversely proportional to the propagation delay of single stage inverter, a considerable improvement in output frequency can be observed. The skewed scheme is effective in RO with CMOS inverters due to complementary behavior of transistors. Since oxide TFTs lack stable complementary (p-type) type transisors, it is challenging to adapt skewed scheme in conventional RO with diode-connected load inverter. Pseudo CMOS with bootstrapped load inverter mimics a CMOS inverter and ensures complete rail-to-rail operation. Therefore, pseudo CMOS with bootstrapped load inverter is slightly modified to design the

proposed RO using negative skewed delay scheme. In addition, the oscillator is made programmable such that the frequency of oscillations can be tuned to different frequency range. The programmability is achieved using control bits that set the load capacitance of each inverter, which directly controls the propagation delay and hence, oscillation frequency of RO.

The rest of the paper is organized as follows: Section II gives an overview about fabrication and modeling of IGZO TFTs; section III describes the proposed programmable ring oscillator and the simulated results are presented in section IV. Finally, conclusions are drawn in section V.

II. Device Fabrication and Modelling

Staggered bottom-gate IGZO TFTs, with top contacts, were fabricated on a glass substrate. Gate and source/drain electrodes of 60 nm thick Molybdenum (Mo) layer were sputtered and patterned by photolithography and dry etching. A 100 nm thick multi-layer multi-component dielectric using SiO_2 and Ta_2O_5 was deposited and patterned similar to gate and source/drain electrodes. Next, a 40 nm thick amorphous IGZO semiconductor with a composition of In:Ga:Zn=2:1:1 (atomic ratio) [19] was sputtered to form the channel layer. Towards the end, all devices were annealed at 180 °C for 10 minutes in air. Once the devices were fabricated, the TFTs were characterized to obtain different device parameters. The mobility and oxide capacitance of the device were reported to be around 13.8 $cm^2/V.s$ and 54 nF/cm^2 from measurements, respectively. In-house IGZO TFT model [20] was used to simulate circuits reported in this paper.

III. High-Speed Programmable Ring Oscillator

A. High Speed RO

Negative skewed delay scheme, proposed in [18], is the simplest way to obtain high frequency of oscillations in RO by prematurely turning on/off one of the transistor in an inverter to speed up the transitions between ground and supply rails. Due to the absence of stable p-type transistors in oxide-TFTs, it is challenging to adapt the negative skewed delay scheme directly into the conventional RO with diode connected load based inverter. This is because providing negative delay to the input of driver transistors, to switch them on/off prematurely, will not reduce delay of an inverter stage as gate of load transistor is connected to power supply voltage. Therefore, transistors of diode connected load inverters in conventional RO, cannot be skewed using negative skewed delay scheme to obtain high frequency of oscillations. In order to take advantage of negative skewed delay scheme, inverter which can mimic a CMOS counterpart is required. Pseudo-CMOS inverter using oxide TFTs reported in [21] can be an option, however, in order to obtain complete rail-to-rail operation two different supply voltages are needed.

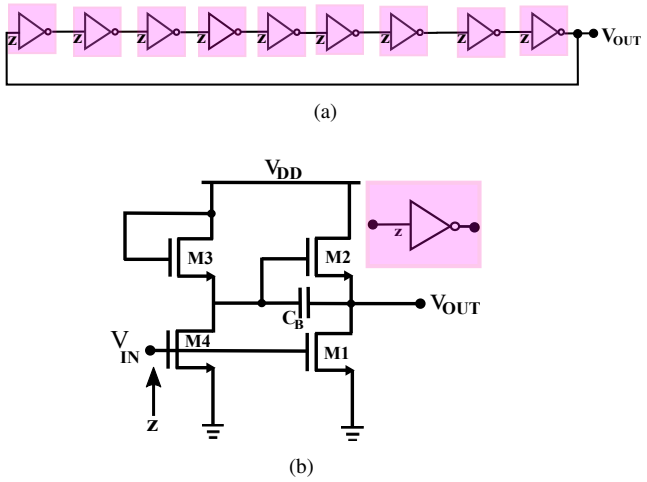

Fig. 1. (a) Block diagram of 9 stage RO (b) Pseudo-CMOS inverter with Bootstrapped load.

Pseudo-CMOS inverter with Bootstrapped load [16] mimics a CMOS inverter and provides rail-to-rail operation without using additional power supply voltage. Fig.1(a) shows the block diagram of 9 stage RO with Pseudo-CMOS bootstrapped load inverter, whose schematic is presented in Fig.1(b). In this inverter, bootstrapped capacitor, C_B, is responsible for boosting output voltage to supply voltage, V_{DD}, when logic 0 is applied to the input of inverter. On the other hand, when logic 1 is applied at the input, $M2$ can be turned off completely through $M4$ (typically $W_{M4} \geq W_{M3}$ and the V_{DSM4} is close to 0 V) which ensures rail-to-rail operation.

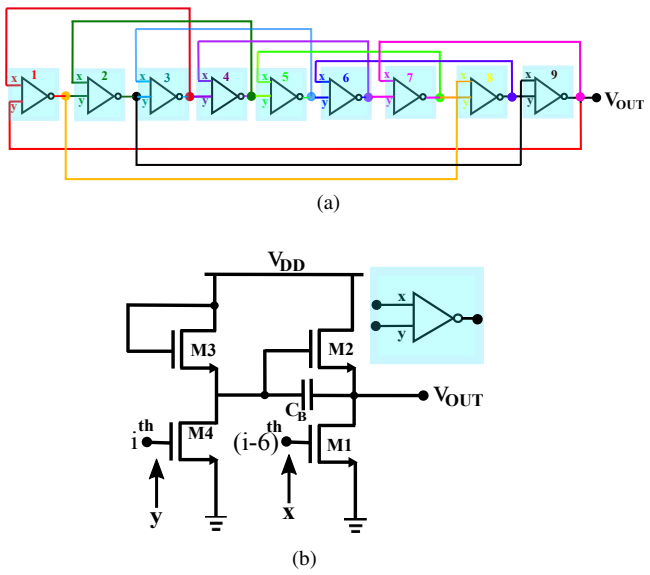

Fig. 2. (a) Proposed high speed 9 stage RO (b) Modified architecture of pseudo-CMOS inverter with bootstrapped load for proposed RO.

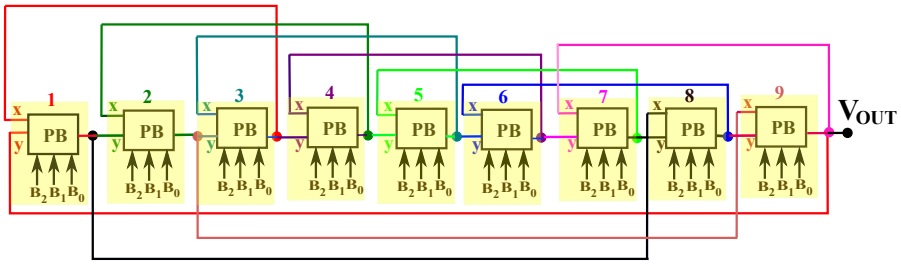

Fig. 3. Proposed High Speed 9 stage programmable RO.

Fig.2(a) shows the block diagram of proposed high speed RO using negative skewed delay scheme. In this architecture, pseudo-CMOS inverter with bootstrapped load is modified slightly. As shown in Fig.2(b), gate of transistors M1 and M4 are separated as x and y, respectively, which are connected to the output of $(i-6)^{th}$ stage and i^{th} stage (for this particular case), respectively. This ensures premature triggering of M1 as x arrives earlier than y (Fig.2(b)), which in turn reduces the propagation delay of each inverter leading to high frequency of oscillations. In addition to high speed of operation, almost rail-to-rail swing can be ensured.

B. Programmable High Frequency RO

The high speed RO discussed in the previous subsection is made programmable in order to tune oscillator frequency over different frequency range. Frequency of oscillation, f_{clk}, of n-stage RO, is given by:

$$f_{clk} = \frac{1}{2.n.T_{delay}} \tag{1}$$

Here, T_{delay} is propagation delay of an inverter in RO. The propagation delay introduced by each stage is proportional to the load capacitance. Fig.3 shows the block diagram of proposed high speed programmable RO. Here, the inverters are replaced by programmable blocks (PB) which are controlled by bits B_2 (MSB), B_1 and B_0 (LSB).

Three binary weighted load capacitors controlled by three bits, B_2, B_1 and B_0, are connected at the output of inverter (of Fig.2(b)), as shown in Fig.4(a), to program the oscillator frequency. The load capacitance of an inverter is given by:

$$C_{load} = C(2^2B_2+2^1B_1+2^0B_0) = 4CB_2+2CB_1+CB_0 \tag{2}$$

From (2), it can be observed that whenever bits are set to logic high level, its corresponding capacitor is added to increase the load capacitance of an inverter. This increases the propagation delay and hence, reduces frequency of oscillation according to (1). C is the unit capacitor in (2),whose value should be selected carefully, especially when this approach is adopted for negative

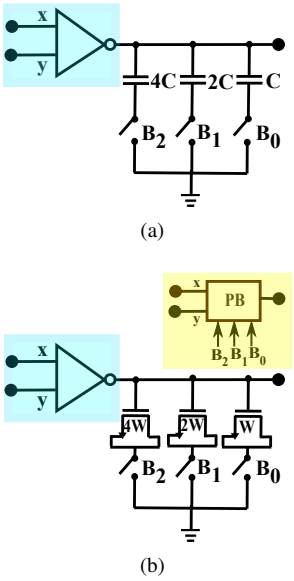

Fig. 4. Programmable block with (a) MIM capacitors (b) MOSCAPs.

skewed delay scheme. High value of C will cause excessive delay and make skewed operation difficult. Therefore, value of C is selected close to parasitic capacitors of the inverters in order to avoid any non-linearity in the operation of negative skewed delay RO. As a result, binary weighted capacitors can be realized using MOS capacitors (MOSCAPs), formed by n-type IGZO TFTs, whose widths are in the ratio 4:2:1 as shown in Fig.4(b) with same channel length. The schematic of Fig.4(b), hence, act as PB for proposed high speed programmable RO shown in Fig.3

IV. Results and Discussions

Circuit simulations have been carried out in Cadence Virtuoso using in-house IGZO TFT model at a supply voltage and device channel length of 10 V and 10 μm, respectively. First, in order to validate 9-stage high speed RO, conventional ROs with diode connected load inverter and pseudo CMOS bootstrapped load inverter have been designed and simulated on the same platform as that of 9-stage high-speed RO. The aspect ratios of the transistors used in different design for simulations are shown in

TABLE I. ASPECT RATIOS OF TRANSISTORS USED FOR SIMULATION OF DIFFERENT ROS

ROs		Width (μm)	Length (μm)
With Diode-connected Load Inverter	Driver	320	10
	Load	40	10
With Pseudo-CMOS bootstrapped Load	M2, M1	160	10
	M3, M4	40	10
Proposed	M2, M1	160	10
	M3, M4	40	10

Table 1. In addition, the bootstrapped capacitor, C_B, for pseudo bootstrapped load inverter, is kept as 5 pF.

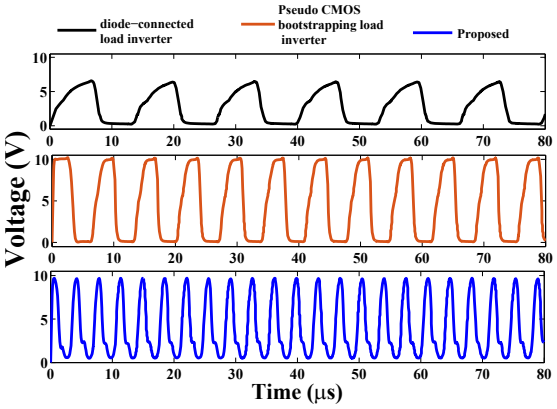

Fig. 5. Simulation Results of conventional and high-speed 9 stage ROs.

From the simulation results, shown in Fig.5, it can be observed that the high-speed RO, designed using negative delay skewed scheme, offers high frequency of oscillations compared to other conventional design. Table II summarizes performance metrics of high-speed RO and compares it with conventional ROs in terms of power, output swing and frequency of oscillations. It can be noticed that the proposed RO provides 95.3% improvement in frequency of oscillations with 33.4% more power consumption compared to conventional RO with pseudo-CMOS bootstrapped load. As a result, power delay product is improved by proposed high speed RO (see Table II).

The high-speed RO is made programmable using external bits, B_2, B_1 and B_0 and MOSCAPs with binary weighted widths as explained in the previous section. The widths of MOSCAP transistors are selected as 40 μm, 20 μm and 10 μm corresponding to bits B_2, B_1 and B_0 for a channel length of 10 μm. Three programmable bits give 8 different frequencies of oscillation ranging from 241.2 KHz to 283 KHz as shown in Fig.6 with a step size of almost 6 KHz. From the figure, almost linear decrements in frequency of oscillation can be observed when the load capacitance at the output of the inverter is increased with increase in decimal equivalent values provided by programmable bits. For fine resolution (step size), number of bits can be increased. Fig.7 shows the simulation results of programmable high-speed RO under no load ($B_2B_1B_0$ = 000) and full load ($B_2B_1B_0$ = 111) conditions.

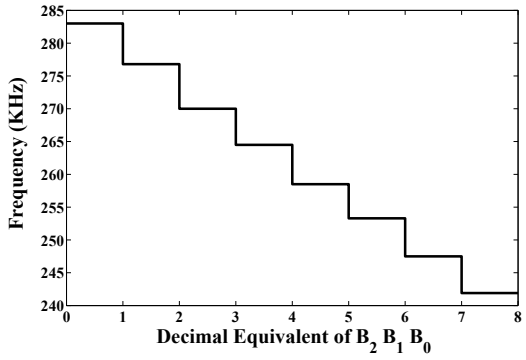

Fig. 6. Staircase showing linearly spaced frequency of oscillations.

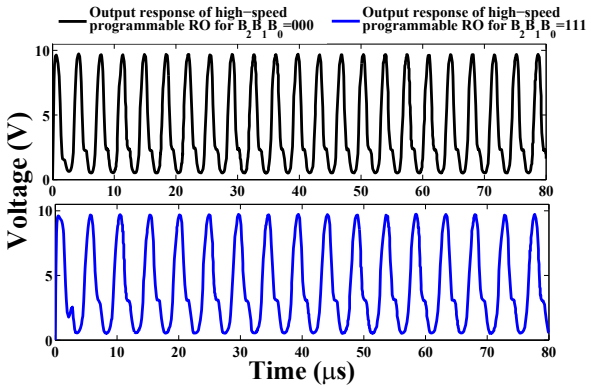

Fig. 7. Simulation result of proposed 9 stage RO.

Table III compares the performance of the proposed oscillator with state of art work. It can be observed that for the first time programability is introduced in RO to obtain different frequency of oscillations. The RO reported in [9]-[14] have poor voltage swing, and therefore are not potential candidate for clock generators. It should be noted that the proposed RO gives better speed compared to RO reported in [15]. The RO in [15] is designed using transistors with a mobility of 36 cm^2/V.s that is almost double the mobility of the transistors used in this work. On the other hand, dual gate transistors are used in [16] which requires additional processing step compared to single gate transistors. In comparison to the state of art work, the proposed circuit is able to provide high speed of operation and almost rail-to-rail output swing, with single gate transistors whose mobility is around 13.8 cm^2/V.s. Speed can be further improved by employing self-aligned structures and devices with high electrical mobility.

V. CONCLUSION

This paper presents a high speed programmable RO with a-IGZO TFTs that can provide 95.3% improvement

TABLE II. PERFORMANCE METRICS OF CONVENTIONAL AND HIGH-SPEED ROS.

9-stage ROs		Power Consumption (mW)	Frequency of Oscillations (KHz)	Output Voltage Swing (V)	Power Delay Product (nJ)
Conventional	**with Diode-Connected Load Inverter**	0.930	76.52	6.05	0.675
	with Pseudo CMOS bootstrapped load inverter	2.069	144.90	10	0.793
Proposed		2.760	283.00	9.2	0.542

TABLE III. COMPARISON OF PROPOSED RO WITH STATE OF ART

*Observed from reported results in state of art

ROs	Stages	Frequency (KHz)	Voltage Swing* (% of supply voltage)	Supply Voltage (V)	Channel length (μm)	Programability
[9]	11	94.8	50	20	11	No
[10]	11	47	60	15	9	No
[11]	11	781	30	20	10	No
[12]	11	810	48.6	25	9	No
[13]	5	2100	0.5	25	10	No
[14]	7	6510	3	20	6	No
[15]	11	132	96	5	10	No
[16]	13	360	100	20	6	No
This Work	9	241.2-283	92	10	10	Yes

in frequency of oscillations compared to conventional RO at cost of 33.4% increment in the power consumption. In addition, for the first time programmability is introduced in the RO to achieve eight linearly spaced oscillation frequencies ranging from 241.2 KHz to 283 KHz with a step size of around 6 KHz with 3 control bits. The proposed RO is able to provide a voltage swing of 92% of V_{dd}. Compared to state of art, this novel RO is able to deliver good performance parameters for a given technology. Hence it would find potential application as on-chip clock generator in smart packaging and wearable devices.

ACKNOWLEDGMENT

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