

A Low-Power Rail-to-Rail Row/Column Selector Operating at 2 V Using a-IGZO TFTs for Flexible Displays

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Abstract—This paper presents design and implementation of 8-bit shift register with low-voltage amorphous Indium Gallium Zinc Oxide (a-IGZO) thin-film transistors (TFTs) for row/column selection of pixel matrix in flexible displays. This circuit is capable of ensuring complete rail-to-rail operation by employing novel NAND gates that were developed based on capacitive bootstrapping load. As a first step, a positive edge triggered D- flip flop (D-FF) is designed using these logic gates, then a complete 8-bit shift register is designed and simulated using in-house low-voltage IGZO TFT models in Cadence Virtuoso. During these circuit simulations a power supply voltage of 2 V and a channel length of $2\ \mu\text{m}$ were used. Simulation outcome of 8-bit shift register has shown a power consumption of $72.15\ \mu\text{W}$ with output voltage swing of 95% of V_{dd} at 20 kHz operating frequency, going well beyond the state of the art for oxide TFT technology at very low supply voltage. The proposed circuit can be used as a row/column selector in flexible displays that can operate at low supply voltage and allows small active-area.

Index Terms—IGZO TFTs, pseudo-CMOS, capacitor bootstrapping, shift register, low-voltage operation.

I. INTRODUCTION

A-IGZO TFTs are gaining significant interest in next generation flexible displays [1], as they can be fabricated at low-temperature (typically around 150°C) [2][3], have high mobility ($\approx 10\ \text{cm}^2/\text{V.s}$) and stability compared to other TFTs (like a-Si:H, organic). Traditionally, drivers for displays are fabricated using CMOS technology, either using assembled Si chips or on-panel circuitry based on low-temperature poly-Si (LTPS) [4] technology due to high field-effect mobility of charge carriers in comparison to other TFT counterparts, to ensure high speed of operation. However, even for LTPS, fabrication temperature is typically above 400°C , due to which conventional process used for fabricating LTPS TFTs on glass substrate cannot be adopted on flexible substrate [5]. As a consequence, oxide TFTs are preferred choice

for flexible displays in which shift registers are important functional blocks for row/column selection.

The works reported so far on shift registers with oxide TFTs [8]- [11] include a power supply $\geq 8\text{ V}$ and transistor channel length $\geq 10\ \mu\text{m}$. High operating voltages and large device dimensions of oxide TFTs impose limitation on the implementation of low-power flexible small displays for specific applications, such as, smart-watch displays, micro display applications, pico-projectors etc. with high pixel density. In order to ensure low-power consumption and small area of overall display, it is essential to optimize the power consumption and active area of the display drivers (shift registers). This can be obtained by scaling down the supply voltage and transistor dimensions. On the other hand, oxide TFTs with a channel length $\leq 8\ \mu\text{m}$ show short channel non-idealities, which degrades the circuit performance [12][13]. Regarding operating voltage of oxide TFTs, it is limited by the rather thick ($> 100\ \text{nm}$) and low-k (3.9 for SiO_2) insulators typically used when low-temperature fabrication is envisaged. In addition, this technology lacks stable reproducible complementary type device (p-type), hence circuit design has to be accomplished only with n-type transistors.

In order to develop a low-power and miniaturized shift register, this paper proposes an 8-bit shift register that can address all the afore mentioned challenges. The circuit is implemented using cascade stages of positive edge triggered D-FFs, which are designed using NAND gates. With the use of only n-type transistors in NAND gate, complete rail-to-rail operation at the output is quite challenging to achieve. Therefore, novel NAND gate with modified capacitive bootstrapping load has been used in order to ensure complete rail-to-rail operation of 8-bit shift register. Due to low supply voltage (2 V) and small channel length of transistor that were employed in the

circuit ($2\ \mu\text{m}$), the power consumption and active area of the proposed circuit is optimized.

The rest of the paper is organized as follows. Section II gives a brief introduction about low voltage a-IGZO TFT devices and model that is used for designing and simulating the proposed circuits. Section III presents logic gates that were previously reported with only n-type transistors and their limitations. Section IV presents design aspect of novel NAND gate, positive edge triggered D-FF and 8-bit shift register. Section V shows the simulation results of the gates, D-FF and 8-bit shift register at a supply voltage of 2 V, using oxide TFTs with channel length of $2\ \mu\text{m}$. Finally, section VI draws conclusions.

II. LOW VOLTAGE A-IGZO TFT: FABRICATION, CHARACTERISTICS AND MODELING

The staggered bottom-gate a-IGZO TFTs were fabricated on a glass substrate in order to extract electrical measurements and create a representative device model. A 60 nm Mo layer was deposited, by means of RF magnetron sputtering, to form gate, source and drain electrodes. A far-ultraviolet assisted process allow spin-coating of 20 nm thick AlO_x dielectric layer, using combustion synthesis process with a solution based on aluminium nitrate precursor. More details on this insulator can be found in [14]. For patterning layers, optical photolithography and dry (Mo) or wet (IGZO and AlO_x) etching processes were used. Finally, all the devices were annealed at 180°C , in air, for 1 hour.

Fig.1(a) shows SEM image of a-IGZO TFT fabricated with a width and length of $55\ \mu\text{m}$ and $2\ \mu\text{m}$, respectively. The drain source overlap with the gate is also visible in light shade around the gate metal ($\sim 2.5\ \mu\text{m}$ on each side). The effective length of the transistor is shown in the inset. Device measurements (I-V and C-V) have

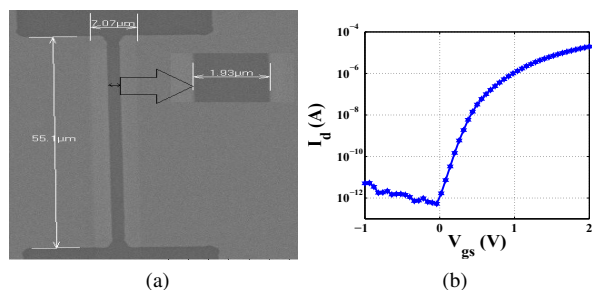


Fig. 1. Low voltage a-IGZO TFT (a) SEM with width of $55\ \mu\text{m}$ and length $2\ \mu\text{m}$ (b) Transfer Characteristics for V_{gs} swept from -1 V to 2 V at $V_{ds}=2\ \text{V}$.

been carried out under dark at room temperature using a Keysight B1500A semiconductor parameter analyzer and a Cascade EPS-150 microprobe station. The transfer characteristics from the measurement is shown in Fig.1(b)

when the gate voltage (V_{gs}) is swept from -1 V to 2 V with a step size of 0.06 V at $V_{ds}=2\ \text{V}$. The output and C-V characteristics, from measurements, are presented in Fig.2(a) and Fig.2(b), respectively. For the output

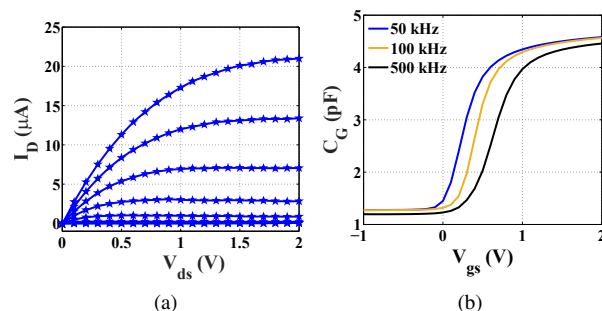


Fig. 2. Low voltage a-IGZO TFT (a) Output Characteristics when V_{gs} is swept from 0 to 2 V with a step size of 0.25 V (b) C-V Characteristics for different frequencies of input signal.

characteristics, V_{gs} is swept from 0 to 2 V with a step size of 0.25 V. It can be observed from the output characteristics that the channel length modulation is not significant even at a small channel length of $2\ \mu\text{m}$, unlike other works reported in [12][13]. Use of a thin AlO_x layer as a dielectric results in a large gate capacitance ($C_{ox}=350\ \text{nF}/\text{cm}^2$), allowing operation of the transistors at a supply voltage of only 2 V (i.e., transconductance saturation until this voltage). From the measurements, extracted field-effect mobility is $14\ \text{cm}^2/\text{V}\cdot\text{s}$. The behavioral modelling of low-voltage a-IGZO TFT, for simulation and designing, is done using artificial neural network based equivalent circuit approach [15] in which parameters extracted from the measurements are used.

III. BASIC LOGIC GATES WITH N-TYPE TRANSISTORS

A. Conventional logic gates

Due to lack of stable complementary type transistor (p-type) with oxide TFTs, circuits need to be designed only with n-type transistors. In this case, the load has to be implemented with either passive resistor (refer Fig.3(a)) or a diode connected transistor (refer Fig.3(b) and Fig.3(c)). Resistive load results in large active area

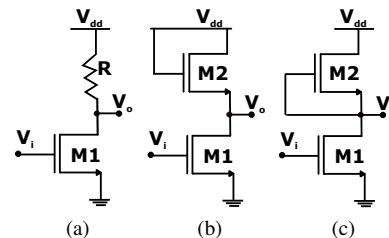


Fig. 3. Inverter with: (a) Resistive Load (b) Diode connected load (c) Zero-bias load.

and high power consumption, therefore, is not a preferred choice for circuit design. The approach of Fig.3(b) results in a threshold voltage drop across the diode load, which in turn limits the output voltage swing and hence, reduces noise margin. Unless M1 is much wider than M2, it is challenging to obtain V_{OL} close to 0V. The zero- V_{gs} architecture, in Fig.3(c) with depletion load, can be a solution to this problem, but it requires extra processing steps to fabricate transistors with different turn-on voltages on the same substrate.

B. Logic gates with Pseudo-CMOS

A pseudo-CMOS based circuit presented in [16] is shown in Fig.4(a). It is capable of providing rail-to-rail output voltage with an additional power supply voltage source, V_{dd1} whose value should not be less than $V_{dd} + 2V_{th}$. Considering all the transistors in pseudo-CMOS inverter circuit to be identical, the operation of the circuit is as follows: When the input voltage, V_i is low (logic 0), transistor M1 turns off and, therefore, the intermediate node X is charged to $V_{dd1} - V_{th}$ which is at least V_{th} more than V_{dd} . As a result, M4 turns on and output voltage, V_o pushes to V_{dd} . On the other hand, when V_i is high, the transistor M1 is on and pulls node X close to logic 0 which turns off M4 while M3 pulls V_o to logic 0. Thus, rail-to-rail operation can be observed. The major limitations of this circuit are the need of more than one power supply voltage source and extra area consumption.

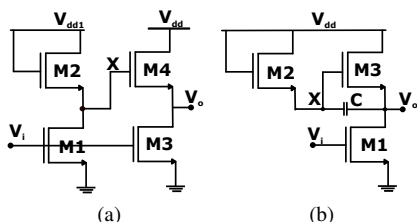


Fig. 4. Inverter with: (a) Pseudo CMOS using two different power supplies (b) Bootstrapping Capacitor.

IV. 8-BIT SHIFT REGISTER WITH NOVEL NAND GATES

Shift registers are implemented by cascaded stages of positive edge triggered D-FFs, which are designed using NAND gates. Different circuits for logic gates have been reported in previous section, but all have limitations either on electrical response or design/fabrication complexity. In order to have rail-to-rail operation and simplicity at circuit and fabrication level, novel NAND gates designed using a modified version of capacitive bootstrapping load are reported. The details of the design for NAND gates, positive edge triggered D-FF and shift register are discussed next.

A. Logic gates with modified capacitive bootstrapping load

Bootstrapping capacitor, C, in logic gate, (as shown in Fig.4(b)) can shift the voltage level at intermediate node X, such that, V_{dd} can be observed at the output when input voltage is logic 0. Thus, eliminating need of second power supply voltage. However, the circuit is not able to drive output completely to zero, when logic 1 is applied to the input due to finite output impedance offered by M3 at low supply voltages. Therefore, Capacitive bootstrapping circuit is modified by adding a switch, for every input, to the bootstrapping inverter such that node X can be pulled down to zero when logic 1 is applied at the input. This will ensure complete rail-to-rail operation. Each switch in the modified circuit is realized using n-type transistor, like M1, which is shown in Fig.5(a). The same technique can be adapted to other logic gates and a 2-input NAND gate with similar implementation is presented in Fig.5(b). With the optimized fabrication process used in this work, Fig.5(a) resulted in a layout area of $5840 \mu\text{m}^2$ when C value is 2.5 pF, which is almost 35.47% of area consumed by pseudo CMOS inverter reported in [16].

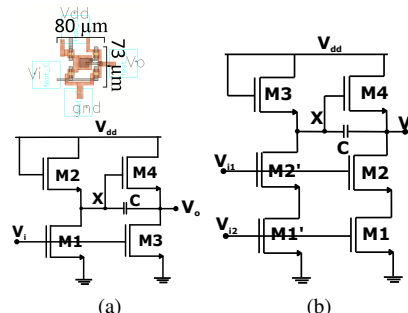


Fig. 5. Logic gates with Modified capacitive bootstrapping load: (a) Inverter: circuit schematic and layout (b) 2-input NAND gate.

B. Positive edge-triggered D Flip-flop

A positive edge triggered D flip-flop (see Fig.6)

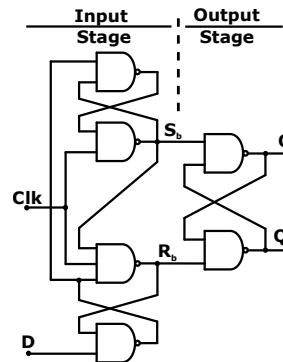


Fig. 6. Positive edge triggered D-Flipflop using NAND gates.

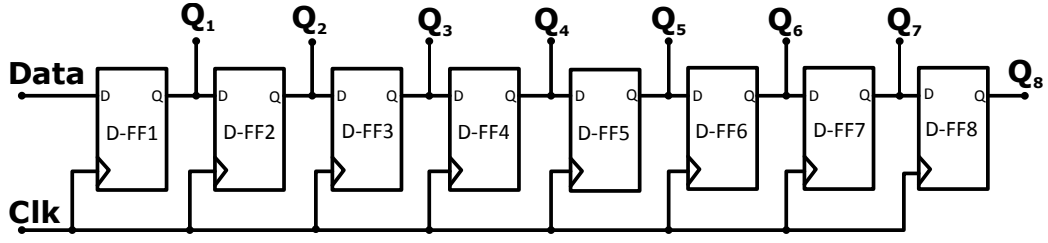


Fig. 7. 8-bit Shift register.

is designed using novel NAND gates whose circuit schematic is presented in Fig.5(b). The operation of the circuit is as follows: The circuit consist of two stages, input and output, implemented by NAND based latches. When the clock (clk) is logic 0, S_b and R_b are set to logic 1. Irrespective of the value of D , Q and Q_b hold previous state. On the other hand, when the circuit comes across a positive edge of the clk , D value will be transferred to Q .

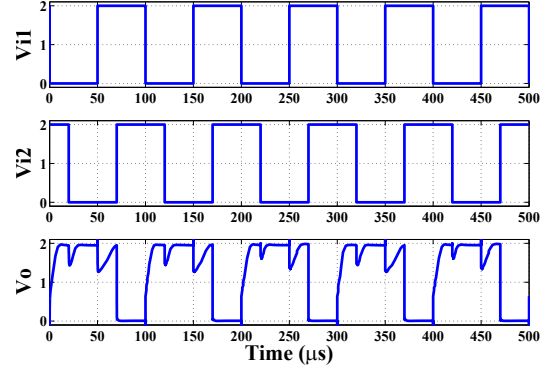
C. 8-bit Shift register for Flexible Displays

As discussed earlier, shift register plays an important role as a row/column selector in flexible displays. An 8-bit synchronous shift register using positive edge triggered D-FFs is presented in Fig.7. For every positive edge of the clk , the output of the shift register shifts by one bit towards right.

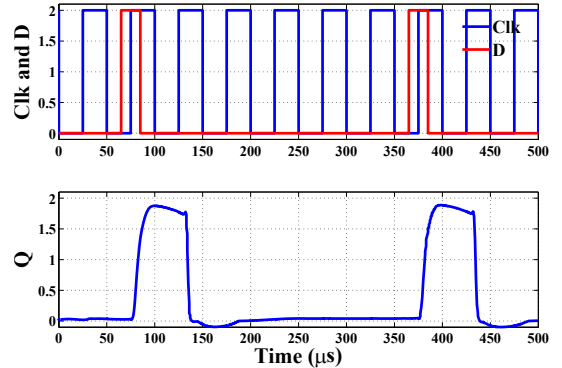
V. RESULTS AND DISCUSSIONS

All the circuit simulations are carried out using low voltage in-house models [15] at a supply voltage of 2 V and a transistor channel length of $2\ \mu\text{m}$, in Cadence Virtuoso. Fig.8(a) shows complete rail-to-rail operation of a 2-input novel NAND gate. Here, the charging and discharging effects at input signals transitions are due to the parasitics of the TFTs. Expected behaviour of positive edge triggered D-FF and 8-bit synchronous shift register can be noticed from Fig.8(b) and Fig.9, respectively. A V_{OH} of 1.9 V and V_{OL} of 0 V have been achieved for both circuits. The 8-bit shift register is showing a power consumption of $72.15\ \mu\text{W}$ at 20 kHz operating frequency with a bootstrapping capacitor of 2.5 pF.

Table I summarizes performance metrics of the 8-bit shift register and compares it with state of art work. Compared to other shift registers reported in literature it can be observed that the proposed circuit consumes considerably less power and works with lower supply voltage, without compromising the operating frequency. In addition, the proposed circuit consumes less area compared to state of art work when the comparison is made at inverter level.



(a)



(b)

Fig. 8. Simulation results of (a) Two input NAND gate. (b) Positive edge-triggered D-FF.

VI. CONCLUSION

This work presented an 8-bit low-power rail-to-rail shift register that is implemented with modified capacitive bootstrapping load based NAND gates for flexible displays. The circuit design makes use of short channel oxide TFTs with a ultra thin solution processed dielectric. This enables low voltage operation (2 V) and low power consumption ($72.15\ \mu\text{W}$), well beyond the previous reports of shift registers with oxide TFTs. This circuit finds potential application in low-power flexible displays with high pixel density, without requiring temperatures above

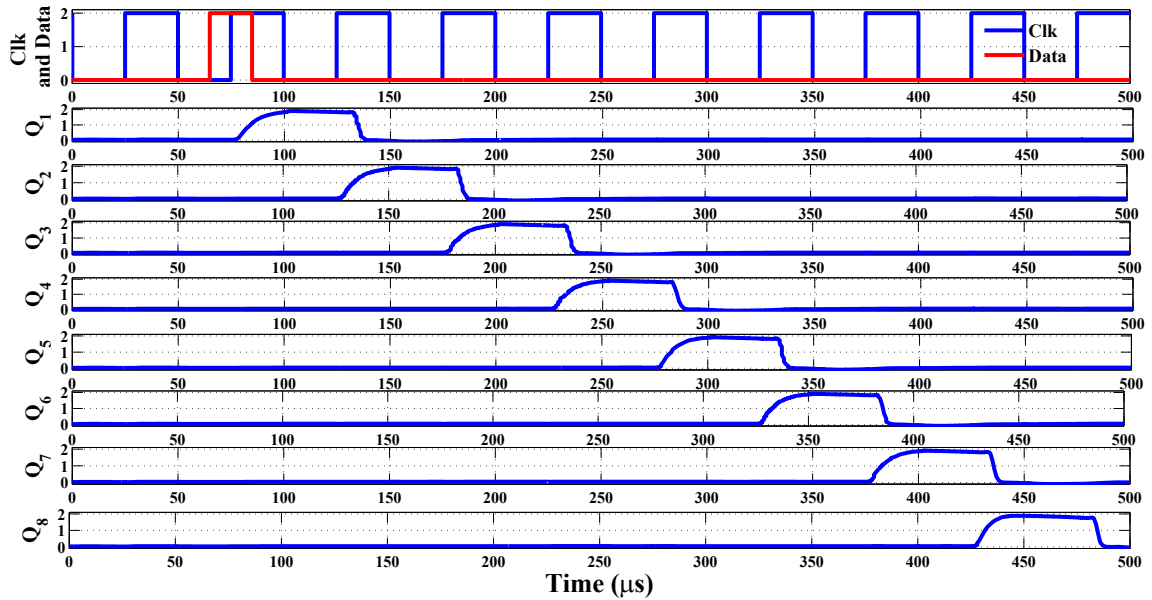


Fig. 9. Transient simulation of 8-bit shift register.

TABLE I
PERFORMANCE COMPARISON OF STATE OF THE ART SHIFT REGISTERS USING OXIDE TFTS

Parameters	[6]	[7]	[8]	[9]	[10]	[11]	This work
Supply Voltage, V_{dd} (V)	20	20	30	2	26	≥ 20	2
Operating Frequency (kHz)	40	13.9	13.2	5	22.1	upto 0.24	20
Device Channel Length (μm)	10	10	10	10	11	11	2
Power Consumption (μW)	-	1670	3800	-	-	-	72.15

180° C for fabrication.

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