A Voltage Controlled Oscillator Using IGZO Thin-Film Transistors

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***Abstract*—This paper presents a voltage controlled oscillator (VCO) using amorphous Indium Gallium Zinc Oxide (a-IGZO) thin-film transistors (TFTs). This circuit consists of a high-gain OpAmp, a comparator and a relaxation oscillator. The implemented relaxation oscillator shows a power consumption of 700 μW, when it is simulated with a supply rails of $\pm$5 V. It shows a frequency of oscillation range from 327 to 560 Hz, when the tuning capacitance value is in varying from 1.6 to 5 pF. On the other hand, the VCO has a power dissipation of 1.3 mW with frequency ranging from 400 to 556 Hz with a controlling voltage from -5 to 5 V. In-house oxide TFT model is used for circuit simulations in Cadence environment. This circuit would find potential applications in large-area flexible systems, namely smart packaging, biomedical and wearable systems, which needs clocks with different frequencies.**

***Keywords*—Relaxation Oscillator, a-IGZO TFTs, comparator with oxide TFTs, positive feedback operational amplifier.**

I. Introduction

Amorphous Indium Gallium Zinc Oxide (a-IGZO) thin-film transistors (TFTs) are gaining significant interest in various real-world applications including smart packaging, biomedical and wearable systems due to their low-temperature fabrication [1], relative high mobility (>10cm^2/V.s) and the stability compared to the other competing low-temperature TFT technologies (a-Si:H and organic TFTs). However, these technologies impose challenges in circuit design due to the absence of a stable complementary device.

In order to ensure compact flexible systems, all the circuits need to be on-chip to eliminate external interface problems. On-chip clock generator is one of the important functional block with frequency of oscillation tuning ability. Though many ring oscillators were reported with IGZO TFTs, they have the limitation of inferior swing, very high supply voltages ($\geq$ 15 V) and a single frequency of oscillation [2], [3], [4], [5]. Nevertheless, a ring oscillator with almost full swing is reported with bootstrapping load, this circuit is also limited to a single frequency of oscillation [6].

In order to address the above mentioned challenges, this work proposes a voltage controlled oscillator (VCO) using IGZO TFTs that contains an OpAmp, a comparator and a relaxation oscillator. Since there is an absence of stable and reproducible p-type oxide TFT, CMOS design techniques cannot be adapted directly, and all desired circuit blocks are to be designed only with n-type transistors. As a first step, an OpAmp and a comparator are designed and characterized. Then the relaxation oscillator and VCO are implemented and simulated using an in-house oxide TFT model [7] in Cadence environment. It should be noted that the model is capable of predicting the circuit behavior very close to the measured response, when the circuit is fabricated under same conditions as the TFTs, whose data was used for model development [7].

The rest of the paper is organised as follows. Section II demonstrates the proposed circuit design and its operating principle. Section III presents the simulation results and discussions and finally the conclusions are drawn in section IV.

II. Circuit Description

The VCO has been implemented as shown in Fig.1. It is comprised of a relaxation oscillator, which is implemented with comparator and an OpAmp. The design of all these circuits with only n-type oxide TFTs are explained as follows.

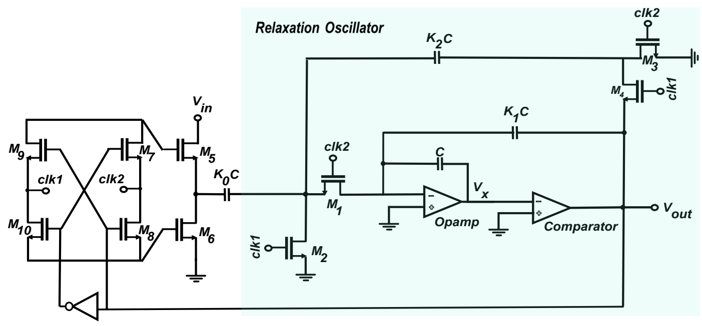

Fig. 1. Circuit diagram of voltage controlled oscillator.

Operational Amplifier: It is an important functional block in the relaxation oscillator circuit and it plays a vital role in minimizing stringent requirements of the comparator design presented in Fig. 1. Circuit schematic of the OpAmp is shown in Fig. 2, where the differential pair formed by transistors M_1-M_4 form a positive feedback loop. The loop gain is A_f as shown in (1). It can be observed that this gain depends on aspect ratios of the transistors forming positive feedback. The aspect ratios of transistors are carefully selected to get the loop gain close to unity. When $A_f \geq 1$, the OpAmp can become unstable [8]. The transistors M_{11} to M_{14} form a differential to single ended converter, which is followed by a common-drain stage.

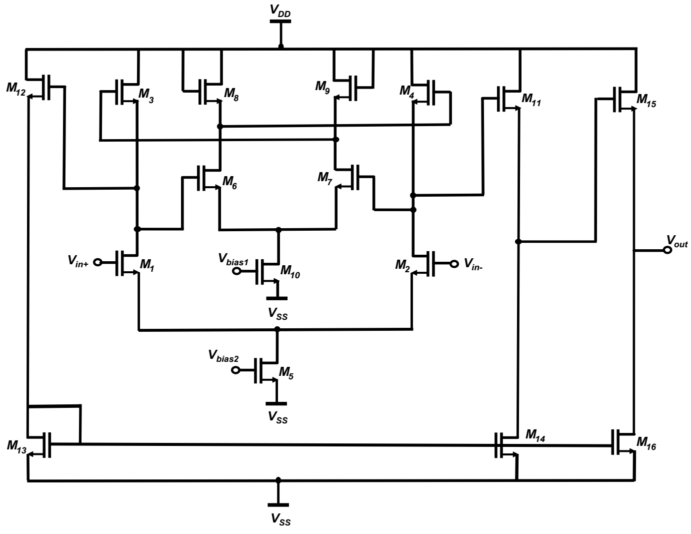

Fig. 2. Circuit diagram of operational amplifier with positive feedback

$$|A_f| = g_{m7}(\frac{1}{g_{m9}||r_{o7}||r_{o9}}) = \frac{g_{m7}}{g_{m9}} \quad (1)$$

The gain of the differential to single ended conversion stage is given by,

$$A_S = g_{m11}(\frac{1}{g_{m11}||r_{o14}||r_{o11}}) \quad (2)$$

and the overall gain of the Opamp is given by,

$$A_v = g_{m1}(\frac{1}{g_{m9}(1-A_f)||r_{o1}||r_{o3}})g_{m11}(\frac{1}{g_{m11}||r_{o11}||r_{o14}}) \approx g_{m1}r_{o1}||r_{o3} \quad (3)$$

Comparator: The architecture of the proposed comparator is shown in Fig.3. In order to ensure faster response, and get rid of clock feed-through and kickback noise, the proposed comparator consists of three preamplification stages and a static latch. Each preamplifier consists of a differential pair with positive feedback as shown in Fig.3a. This stage can ensure high-gain due to the positive feedback even with only n-type transistors, as explained in OpAmp design. A cascade of three such stages relax comparator and latch requirements. A regenerative latch together with preamplification stages can ensure faster response.

A latch is a positive feedback regenerative circuit with cross coupled TFTs as shown in Fig.3b. Its output is a growing exponential function of the differential input as per (4). The outputs of the third preamplification stage are applied as input to the latch. Based on the relative magnitude of these signals and threshold voltage of M_{11} and M_{12}, proper digital rails will be resulted at the output of the latch.

$$V_d(t) = V_d(0).e^{t(g_{m13}-\frac{1}{R_{11}})(\frac{1}{C_{11}})} \quad (4)$$

where V_d(t) is the difference between V_{in-} and V_{in+} of Fig.3b at time t, $V_d(0)$ is initial difference voltage, g_{m13} is transconductance of M_{13} and R_{11} and C_{11} are total resistance and capacitance seen at input of M_{11}.

Relaxation Oscillator: The relaxation oscillator circuit schematic is presented in Fig. 1, which has capacitors K_1C, K_2C and C along with switches, OpAmp and comparator. The switches are controlled by non-overlapping clocks, clk1 and clk2. To understand the working of the oscillator, assume V_{out} is at V_{SS}. A charge of K_2CV_{SS} is stored in capacitor K_2C when clk1 is high. This charge is transferred to capacitor C when clk1 is low and clk2 is high. This makes V_x negative by K_2V_{SS}. If this charge is sufficient enough to drive V_x below zero then the V_{out} is driven to V_{DD}. In the next on-time of clk1, the charge stored on capacitor K_2C is K_2C (V_{SS} + V_{DD}) makes the charge more positive and thus V_x becomes more negative. In the following cycles, the voltage at V_x keeps on charging to zero in the steps of K_2V_{DD}. The frequency of V_{out} is given by (5).

$$f = \frac{K_2}{K_1}\frac{f_{clk}}{2+\frac{V_{SS}}{V_{DD}}+\frac{V_{DD}}{V_{SS}}} \quad (5)$$

where f_{clk} is clock frequency of switching.

Voltage Controlled Oscillator: The relaxation oscillator was used to obtain a VCO as shown in Fig.1. The capacitor K_0C, a feed-in capacitor is controlled in such way that the positive V_{in} adds the charge to C with the same sign of K_2C making V_x reach zero earlier, thus increasing the frequency. With V_{in} the charge added to C has opposite polarity comapared to that of K_2C making V_x reach zero later leading to lower frequency. The frequency of VCO is calculated using (6).

$$f = (\frac{K_2}{4K_1})f_{clk} + V_{in}(\frac{K_0}{4K_1V_{DD}})f_{clk} \quad (6)$$

where V_{in} is voltage that contorls the oscillation of the circuit.

III. Results and Discussion

Using inhouse oxide TFT model the OpAmp, the Comparator, the Relaxation Oscillator and the Voltage Controlled Oscillator have been designed and simulated in Cadence environment with a power supply rails of ±5 V.

The performance of the OpAmp: When the positive feedback operational amplifier shown in Fig. 2 is simulated, it is showing a gain of 61.7 dB. It is stable with a phase margin of 72^0, power consumption of 200 μW and has a unity gain bandwdith of 158 kHz as shown in Fig.4.

The performance of the Comparator: As stated before, the comparator in the work has three preamp stgaes and a latch as shown in Fig. 3. Whereas, Fig.5 shows the gain and phase response of a single-stage preamplifier with a gain of 10 dB and phase margin of 68^o. Fig.6 shows the output response of comparator having a swing of 4.32 to -4.21. Other performance metrics of the comparator are shown in Table I.

The performance of Relaxation Oscillator: The output V_{out} and the intermediate voltage level V_x has been shown in Fig.7. In this response, the output is obtained for a clock

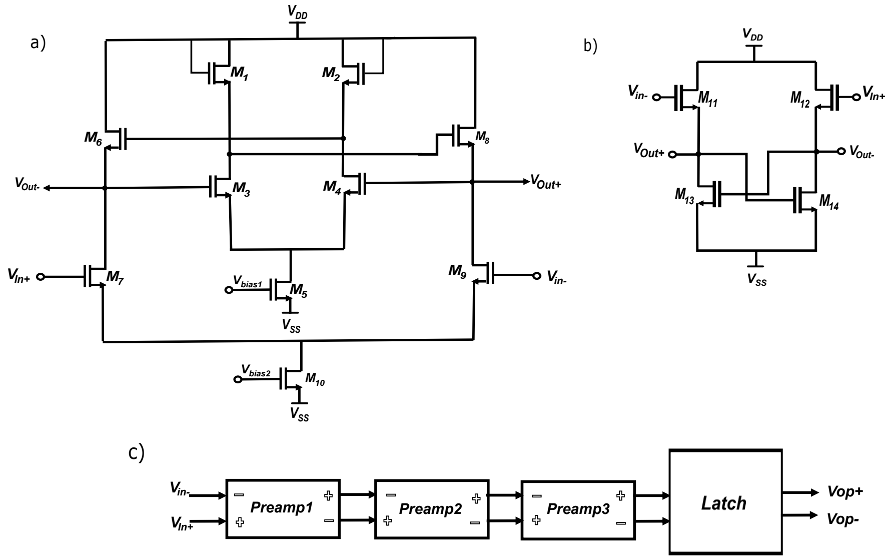

Fig. 3. Circuit diagram of a comparator: a) Preamplifier b) Latch c) Complete Comparator

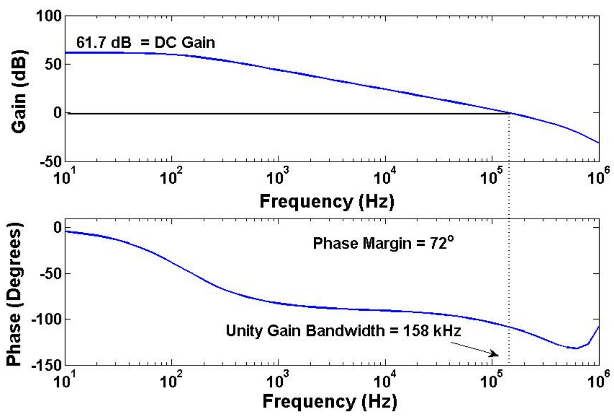

Fig. 4. Response of operational amplifier showing gain and phase plots

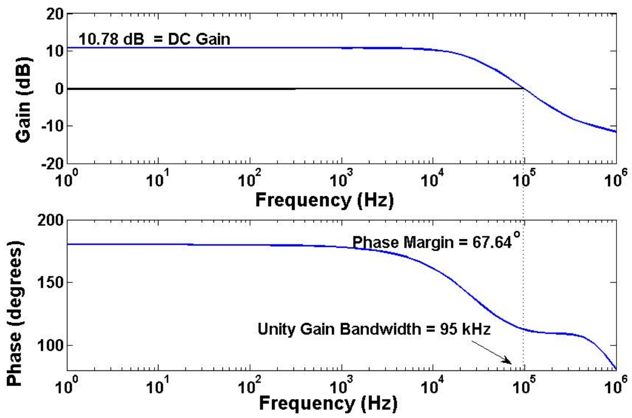

Fig. 5. Response of single stage preamplifier showing gain and phase plots

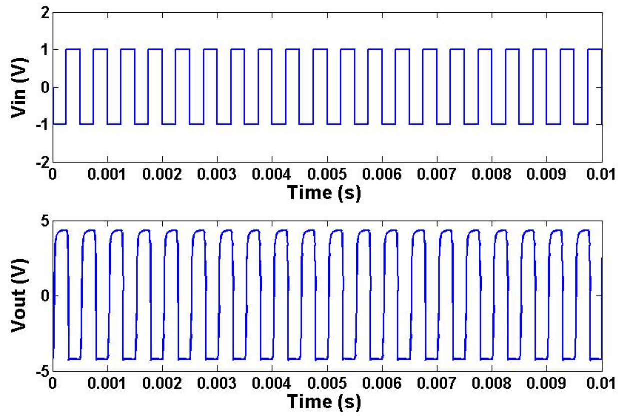

Fig. 6. Output of comparator showing input and output voltages

TABLE I. CALCULATED PARAMETERS OF COMPARATOR

S.NO.	PARAMETERS	VALUES
1.	Systematic offset	60 mV
2.	Slope	22 V/sec
3.	Resolution	50 mV
4.	Power consumption	300 μW

frequency of 10 kHz. The charging and discharging of capacitor C in form of steps with sizes of K_2V_{DD} or K_2V_{SS} can be seen as the voltage V_x.

The relation between the oscillating frequency and capacitor K_2C is linear as shown in (5) from theoretical prediction. The simulated outcome is compared and validated with the expected value in Fig.8. The frequency increases from 327 to 560 Hz with the increase in K_2/K_1 value from 0.08 to 0.24 with K_2C varying from 1.6 to 5 pF and K_1C of 20 pF. There is a slight deviation from predicted frequency because of non-idealities of the opamap and comparator. The proposed

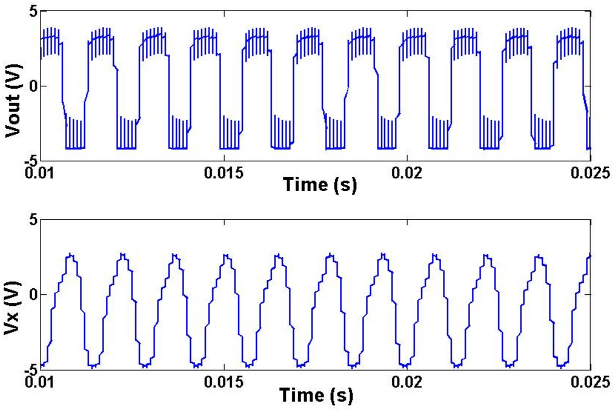

Fig. 7. Output response of relaxation oscillator

relaxation oscillator has a power consumption of 700 μW at 500 Hz. The ratio of clock frequency to oscillation frequency is around 20:1 ratio. With the suitable K_2/K_1 ratio the circuit can also work as frequency divider circuit.

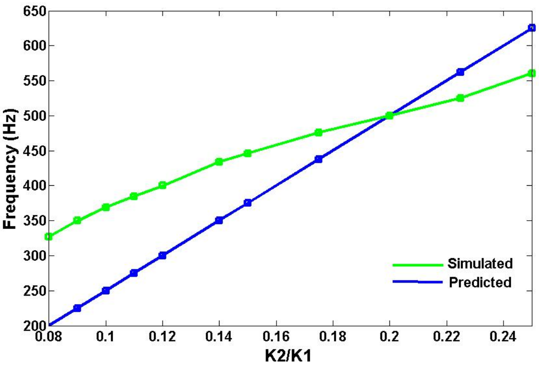

Fig. 8. Plot between the simulated and predicted values of the relaxation oscillator

The performance of the Voltage Controlled Oscillator: The VCO has a power consumption of 1.3 mW. The variation of frequency has a slight deviation from calculated values in Fig.9, due to non-idealities of the devices and circuits. The linearity between the input voltage V_{in} of Fig.1 and the frequency of V_{out} is evident from the graph and is in agreement with (6).

It should be noted that the semiconductor is amorphous in nature and the field-effect mobility is around 10 $cm^2/V.s$. This device inferior performance lead to low frequency of oscillation. Further improvement in the phase noise can be obtained by using design techniques consists of two comparators [9]

IV. Conclusions

This paper presented a voltage controlled oscillator with IGZO TFTs for the first time, which is capable of generating variable frequencies by tuning the voltage. The circuit can be used as on-chip oscillator with frequency tuning ability or as frequency divider (refering to relaxation oscillator) in flexible large-area systems, such as, smart packaging, wearable electronics and biomedical applications.

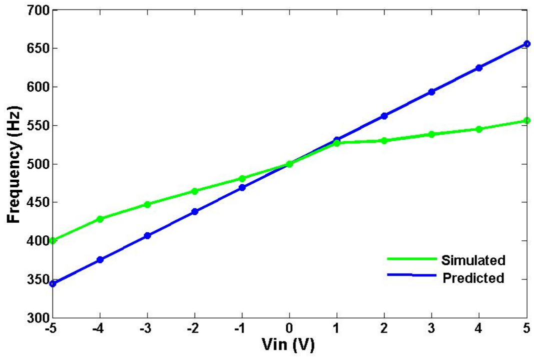

Fig. 9. Plot between the simulated and predicted values of VCO

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